

LT9102 --- Product Brief

MIPI Single-port to MIPI Dual-port Bridge

1. Features

● Single-Port MIPI DSI/CSI Receiver

- Compliant with D-PHY2.1 & DSI 1.1 & CSI-2 2.0
 - 1 clock lane and 1/2/3/4 configurable data lanes per port
 - Up to 4.5Gbps per data lane
- Compliant with C-PHY1.2 & DSI-2 1.0 & CSI-2 2.0
 - 1/2/3 configurable data trios
 - Up to 3.5Gsps per data trio
- Support BTA (Bus Turnaround)
- Support up to 4K@90Hz RGB 8bpc
- Support up to 8K@60 DSC pass-through
- DSI Support 16/20/24-bit YCbCr4:2:2, 16/18/24/30/36-bit RGB, 12-bit YcbCr420, Compressed Pixel Stream
- CSI Support RGB888/666/565, YUV422 8/10bit, YUV420 8bit (legacy), RAW (pass-through)
- Support DSI Video mode
- Support DSI Command mode (pass-through)
- D-PHY support data lane swap and PN swap
- C-PHY support trio swap

● Dual-Port MIPI® DSI/CSI Transmitter

- Compliant with D-PHY2.1 & DSI 1.1 & DSI-2 1.0 & CSI-2 2.0
 - Support 1/2 configurable ports
 - 1 clock lane and 1/2/3/4 configurable data lanes per port
 - Up to 4.5Gbps per data lane
- Compliant with C-PHY1.2 & DSI-2 1.0 & CSI-2 2.0
 - Support 1/2 configurable ports
 - 1/2/3 configurable data trios per port
 - Up to 3.5Gsps per data trio
- DSI Support 16/20/24-bit YCbCr4:2:2, 16/18/24/30-bit RGB, 12-bit YcbCr420, 12Compressed Pixel Stream
- CSI Support RGB888/666/565, YUV422 8/10bit, YUV420 8bit(legacy) , RAW (pass-through)

- Support DSI Low Power Command
- Support side by side and even/odd 3D mode
- Support DSI Video mode
- Support DSI Command mode (pass-through)
- D-PHY support port swap, lane swap and PN swap
- C-PHY support port swap and trio swap
- Support mirror copy on two ports
- Support virtual channel data separation on two ports
- Programmable transmitter swing and pre-emphasis

● OSD

- Support font-based and bit-map OSD
- Support adjustable transparency
- Support Variable Refresh Rate

● Miscellaneous

- CSC: RGB <-> YCbCr4:4:4 <-> YCbCr4:2:2
- Integrated 100/400KHz I2C slave
- Integrated microprocessor
- Internal 25MHz oscillator
- Embedded SPI flash for firmware
- Firmware update through I2C interface
- Power supply: 1.1V and 1.8V

2. General Description

LT9102 is a high performance single-port MIPI to dual-port MIPI bridge chip that supports conversion between DSI and CSI, as well as between D-PHY and C-PHY.

LT9102 can work as a 4-lane/3-trio to 4-lane/3-trio bypass retimer or 4-lane/3-trio to 2*4-lane/3-trio bypass splitter.

LT9102 support converting 4-lane/3-trio to 8-lane/6-trio in L/R mode or Even/Odd mode, which can reduce the mipi datarate by half.

When multiple virtual channel data streams are input via CSI, LT9102 can extract individual VC streams and output them separately through the dual ports.

For MIPI input, LT9102 features single-port MIPI®DSI/CSI

with 1 high-speed clock lane and 1~4 high-speed data lanes operating at maximum 4.5Gbps/lane with D-PHY, which can support a total bandwidth of up to 18Gbps. Also support 3.5Gsps/trio with C-PHY, which can support a total bandwidth of up to 23.94Gbps.

For MIPI output, LT9102 features configurable single-port or dual-port MIPI@DSI/CSI with 1 high-speed clock lane and 1~4 high-speed data lanes operating at maximum 4.5Gbps/lane with D-PHY, which can support a total

bandwidth of up to 36Gbps for dual port. Also support 3.5Gsps/trio with C-PHY, which can support a total bandwidth of up to 47.88Gbps for dual port.

3. Applications

- Mobile system
- Digital video cameras
- Car Display and Camera System

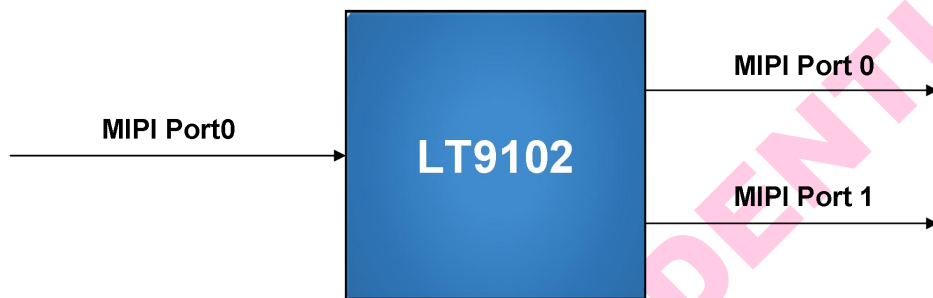


Figure 3.1 Application Diagram

4. Ordering Information

Table 4.1 Ordering Information

Product Name	Part Number	Product Status	Package	MSL	Bonding Wire	Grade	Operating Temperature Range	Stack Die Option	Packing Method	MPQ
LT9102	LT9102_U1Q10CEM	Preview	QFN48 (6*6)Saw	TBD	Cu	E	-40°C to +85°C	M	Tray	TBD

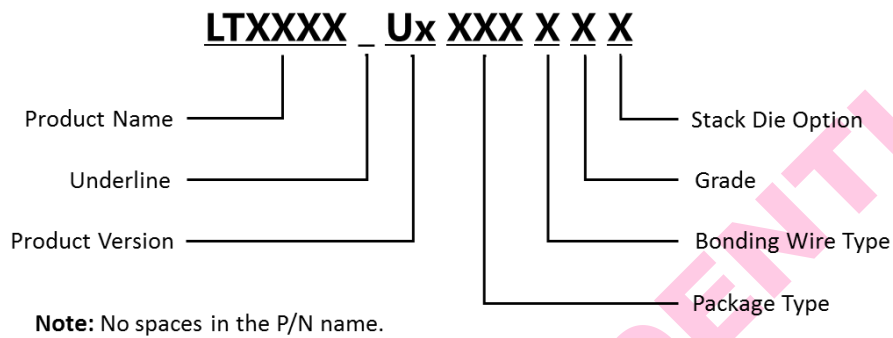


Figure 4.1 Part Number Naming Rules

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